**TESS Memory Requirements**

In order to provide maximum versatility as a general purpose computer, we needed to design a system that would provide a relatively large amount of memory for application use. Therefore, we decided to use off-chip memory resources, and consequently, much of the design of our project was molded around these requirements and their subsequent effects.

An interchangeable socket for ROM would allow a user to swap applications at ease. However, as SRAM is a volatile memory, it was not necessary to swap SRAM chips. Therefore, two different memory chips were selected for modeling our design:

1. EPROM: Atmel AT27C1024-45PU. This chip is a 64k x 16-bit architecture with parallel access of 45ns. This particular chip comes in a 40-DIP package, as to be easily interchangeable on a custom PCB design.
2. SRAM: Integrated Silicon Solution (ISSI) IS61C6416AL-12TLI. This chip is also a 64k x16-bit architecture with parallel access of 12ns. This particular chip comes is 44TSOP package, which will be great for permanent placement on a custom PCB design.

These chips were specifically chosen for both memory size, architecture and access time. While our clock rate is 12.5MHz, we had originally planned a design on a 25MHz clock. This would have required two clock cycles to access the ROM memory, and only one to access SRAM. With the new clock rate of 12.5MHz, both memories can be accessed within the 80ns period of a single clock cycle.

The use off-chip memories was a huge win for chip real-estate, as on chip memory is the main consumer of area. This design decision ultimately allowed us to include other peripheral support beyond just SNES controllers and VGA interface.

While off-chip memories provided the bulk of memory available to the system, it was desirable to have an on-chip, dual ported register file, for the ease of instruction execution and datapath design. While we could have synthesized a register file using our own custom DFF cell design, we opted for using a pre-configured 16x16-bit SRAM design for our register file. This design again mitigated the amount of real-estate consumed by the on-chip memory and allowed for more than enough space for the remainder of the design.